Remarks/Arguments:

By this Amendment, Applicants have amended claims 33 and 34. Claims 1, 4, 6-10, 29-31, and 33-38 are pending.

Claim Rejections Under Section 102

Claims 1, 8, 29, and 36-38 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Patel. Applicants respectfully traverse the Section 102(b) rejection.

Claim 1 is an independent claim to which claims 4, 6-10, 29, and 35-38 depend.

Claim 1 is directed to a semiconductor device and includes the following features:

- a capacitor provided on a supporting substrate and including a lower electrode, a dielectric layer, and an upper electrode, the dielectric layer being formed from a ferroelectric material,
- a first interlayer insulating layer provided as to cover the capacitor,
- a first interconnect selectively provided on the first interlayer insulating layer and electrically connected to the capacitor through a first contact hole formed in the first interlayer insulating layer,
- **a second interlayer insulating layer consisting of an interlayer insulating film having a tensile stress provided on the first interconnect,** and
- **a second interconnect selectively provided on the second interlayer insulating layer** and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating layer.

Applicants submit that the semiconductor device defined by independent claim 1 is patentably distinguished from the Patel Patent at least based on the requirement that the second interlayer

insulating layer consists of an interlayer insulating film having a tensile stress provided on the first interconnect, and a second interconnect selectively provided on the second interlayer insulating layer. Simply put, the semiconductor device of claim 1 requires a second interlayer insulating layer sandwiched between a first interconnect and second interconnect, and further requires that the second interlayer insulating layer have a tensile stress. These features are neither taught nor suggested in the Patel Patent.

The Patel Patent relates in general to a method for forming a ferroelectric capacitor for use in an integrated circuit establishing one layer over another and then annealing the structure, using an oxygen or ozone anneal, after each layer is established.

More specifically, Applicants focus on the planarized intermetal dielectric 28 as shown in Figures 11 and 12 of the Patel Patent, and which is further described in the Patel Patent at column 6, lines 1-17. The Office Action has taken the position that this dielectric 28 is comparable to the feature of the second interlayer insulating layer defined in Applicants' claim 1. Applicants respectfully disagree. Specifically, there is no teaching in the Patel Patent of a second interlayer insulating layer which has a tensile stress, and which is on the first interconnect and which has a second interconnect thereon. In other words, there is no teaching or suggestion in the Patel Patent of a second interlayer insulating layer sandwiched between a first interconnect and a second interconnect, where the second interlayer insulating layer has a tensile stress.

According to the Patel Patent at column 6 the planarized intermetal dielectric 28 can be a sandwich of plasma enhanced chemical vapor deposition of SiH_4 and N_2O (PECVD oxide)/Spin-On Glass (SOG)/PECVD oxide or PECVD oxide/Atmospheric Pressure CVD (APCVD) $TEOSO_3$/PECVD oxide. Patel is therefore disclosing a multi-insulating layer as discussed in column 6, lines 1-17 of the Patel Patent. This is not the same structure of the semiconductor interlayer insulating layer in Applicants' claimed invention which "consists" of an interlayer

insulating film. A further difference is that Patel is disclosing a multi-insulating layer whereas Applicants are defining a single interlayer insulating film.

The Office Action also takes the position that the dielectric 28 has tensile stress as required in Applicants' claim 1. Applicants respectfully disagree. First, there is simply no teaching or suggestion in the Patel Patent that dielectric 28 has tensile stress. In fact, from the description of dielectric 28, Applicants understand that quite the opposite is present and that the dielectric 28 has instead compressive stress. Applicants are of the position that it can not be assumed that dielectric 28 has tensile stress because upper PECVD oxide and low PECVD oxide are provided within the dielectric 28 of Patel and from these it is apparent that the dielectric 28 will have a compressive stress.

Thus, it is Applicants' position that a second interlayer insulating layer being sandwiched between the first interconnect and the second interconnect, and it being of a single interlayer insulating film, and it having tensile stress are features which are simply not taught or suggested in the Patel Patent with respect to the planarized intermetal dielectric 28. For these reasons Applicants respectfully submit that claim 1 and the claims dependent thereon are patentably distinguished from the Patel Patent.

The structural differences noted above between the semiconductor device of Applicants' claim 1 and the disclosure of the Patel Patent are due to the different problems which Applicants invention wishes to solve and the problems which the Patel Patent wishes to solve.

In the Patel Patent, the dielectric 28 is formed by plasma CVD. Such a structure is in contrast to the purpose and disclosure of Applicants' claimed invention. In the subject application in the "Background of the Invention" section, the Applicants identify a new problem not considered by Patel. As Applicants explain in the Background of the Invention, if a plasma TEOS film is used as the second interlayer insulating film 15 on the first interconnect 14, which are provided on a capacitor, a compressive stress acts on a dielectric film 8, preventing a polarization of the dielectric material forming the dielectric film 8. As a result, the physical

properties of the dielectric film 8, formed of high dielectric constant film or a ferroelectric material film, deteriorates. Therefore, the present invention provides a semiconductor device including the second interlayer insulating layer without a plasma TEOS film in order to solve this problem. The Patel Patent, on the other hand, does not consider this problem and does not consider resolution of this problem as have Applicants. Thus, it is not surprising to Applicants that the structure of the semiconductor device defined by claim 1 is different than the semiconductor device described by the Patel Patent.

In view of the foregoing remarks, Applicants request that the Section 102 rejection directed to claims 1, 8, 29, and 36-38 be withdrawn.

Claim Rejections Under § 103

Claims 4 and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Patel in view of Zafer; claims 6 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Patel in view of Hanagasaki; claim 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Patel in view of Applicants' admitted prior art; claims 8, 30, and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Patel in view of Matsuki; and claims 33 and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Patel in view of Arita. Based on this Amendment, Applicants respectfully traverse the Section 103(a) rejections.

As Applicants have pointed out above, there are several features which the Patel Patent simply does not teach or suggest with respect to the second interlayer insulating layer defined in Applicants' claim 1. Claims 30, 31, 33, and 34 are independent claims. With the amendment of claims 33 and 34 by this Amendment, it is Applicants' position that independent claims 30, 31, 33, and 34 include the same features as noted above with respect to claim 1, which patentably distinguish claim 1 from the Patel Patent. Thus, all pending claims include the above discussed features. It is Applicants' contention that the Zafer Patent, Hanagasaki Patent, Matsuki Patent, Arita Patent, and Applicants' admitted prior art do not teach or suggest the

features discussed above with respect to the second interlayer insulating layer, and therefore the combination of any of these references with the Patel Patent will not teach or suggest Applicants' claimed invention as defined in all of the independent claims, and therefore all the dependent claims.

The Zafer Patent in general relates to one or more dielectric layers 32 and 52 formed over a ferroelectric capacitor 24 of a FENVM cell, where the tension within the dielectric layers 32 and 52 overlaying the ferroelectric capacitor 24 is kept relatively low.

The Hanagasaki Patent relates in general to a method of manufacturing a semiconductor storage device having a plurality of memory cells each having one transistor and one ferroelectric capacitor and includes the steps of forming a transistor, forming a plate line, sequentially laminating three layers including a first conductive film, a ferroelectric layer, and a second conductive layer stacked in this order, and sequentially etching the three layers by using a single etching mask.

The Matsuki Patent in general relates to a method of manufacturing a non-volatile semiconductor memory device comprising the steps of forming a ferroelectric capacitor, sputtering a first dielectric film on the ferroelectric capacitor, and depositing a second dielectric film on the first dielectric film by a CVD process.

And the Arita Patent in general relates to a semiconductor device forming a capacitor through an interlayer insulating layer on a semiconductor substrate on which an integrated circuit is formed.

Each of the above noted patents has been cited for a specific reason in the Office Action. But none of them has been cited with respect to the specific features of Applicants' second interlayer insulating layer which patentably distinguishes Applicants' claimed invention from these patents. As for the admitted prior art, it has been cited with respect to a thickness of about 1 μm relative to the second interlayer insulating film. But there is no disclosure in

Applicants' admitted prior art which discusses or suggests the features of the second interlayer insulating layer which patentably distinguish Applicants' claimed invention.

Based on the foregoing remarks, Applicants respectfully request that the Section 103 rejections directed to claims 4, 6, 8, 9, 10, 30, 31, 33, 34, and 35 be withdrawn.

Applicants note that there is no discussion or rejection in the Office Action with respect to dependent claim 7. Applicants would appreciate clarification as to whether the Examiner has found claim 7 includes allowable subject matter, or the basis of any rejection of claim 7.

In view of the foregoing remarks and amendments, Applicants respectfully submit that claims 1, 4, 6-10, 29-31, and 33-38 are in condition for allowance. Reconsideration and allowance of all pending claims are respectfully requested.

Respectfully submitted,

Daniel N. Calder

Daniel N. Calder, Reg. No. 27,424
Attorney for Applicants

DNC/lcf

Dated: June 11, 2004

P.O. Box 980
Valley Forge, PA 19482
(610) 407-0700

The Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

June 11, 2004

Lorraine C. Fox Lorraine C. Fox

LCF_I:\YAO\3950\AMEND09.DOC